CLAIMS

What is claimed is:

1. A circuit board for a stacked package comprising:
   an electrically conductive substrate having a plurality of foldable tabs or delineated surfaces; and,
   a multi-layer interconnection circuit having conductive traces fabricated on one or both sides of said substrate, and one or more attachment sites on one or more of said tabs or delineated surfaces, said attachment sites having terminals for connection to selected traces in said interconnection circuit.
2. A circuit board comprising:
   an electrically conductive substrate;
   a multi-layer interconnection circuit having conductive traces fabricated on one or both sides of said substrate, and one or more attachment sites which include a plurality of attachment terminals with each of said terminals adapted to connect with selected traces of said interconnection circuit, wherein each of said terminals is either a bump or a well filled with solder.
3. The circuit board of claims 1 or 2 wherein said conductive substrate is copper or an alloy of copper.
4. The circuit board of claim 1 wherein each of said attachment terminals is either a conductive bump or a well filled with solder.
5. The circuit board of claims 2 or 4 wherein said solder is indium-based.
6. The circuit board of claims 1 or 2 wherein the minimum pitch of said attachment terminals is 100 microns or less.
7. The circuit board of claims 1 or 2 wherein said multi-layer interconnection circuit comprises interconnecting layers of copper conductors embedded in dielectric material.
8. The circuit board of claim 7 wherein said dielectric material includes Cytop.
9. The circuit board of claims 1 or 2 comprising:
   an electrically conductive substrate which is copper or an alloy of copper;
   a first dielectric layer;
   a first patterned conductive layer including conductive power and signal traces;
   a second dielectric layer;

a second patterned conductive layer including conductive power and signal traces;

a third dielectric layer;

a third patterned conductive layer in the form of a ground plane with feed-throughs for signals and power; and,

a fourth dielectric layer with terminals for attachment to selected traces formed therein.

10. The circuit board of claim 9 wherein some or all of said dielectric layers are Cytop.

11. The circuit board of claim 7 wherein selected ones of said copper conductors are arranged in said dielectric material to form transmission lines having controlled impedance.

12. The circuit board of claim 7 wherein selected ones of said copper conductors are shaped and arranged in said dielectric material to form RF circuits.

13. A high density cable comprising:

an electrically conductive substrate;

a multi-layer interconnection circuit having conductive traces fabricated on said substrate and at least two attachment sites wherein each of said attachment sites includes a plurality of attachment terminals and each of said terminals connects with a selected trace of said interconnection circuit.

14. The cable of claim 13 wherein said attachment terminals are either gold stud bumps or wells filled with solder.

15. The cable of claim 13 wherein said multi-layer interconnection circuit comprises interconnecting layers of copper conductors embedded in dielectric material.

16. The cable of claim 15 wherein selected ones of said copper conductors are arranged in said dielectric material to form transmission lines having a characteristic impedance.

17. The cable of claim 13 wherein the pitch of said attachment terminals is 100 microns or less.

18. The cable of claims 13-17 and including multiple branches of said cable, wherein at least one of said attachment sites is provided in each of said branches.

19. A stacked microelectronic assembly comprising:

an electrically conductive substrate having a plurality of foldable tabs or delineated surfaces;

a multi-layer interconnection circuit having conductive traces fabricated on one or both sides of said conductive substrate and one or more attachment sites on one or more of

said tabs or delineated surfaces, said attachment sites having terminals for connection to selected traces in said interconnection circuit;

a plurality of microelectronic elements attached at said attachment sites using said attachment terminals; and,

wherein at least one of said foldable tabs or delineated surfaces is folded to form a stacked arrangement of said folded tabs or delineated surfaces.

20. The stacked assembly of claim 19 wherein said electrically conductive substrate is copper or an alloy of copper.

21. The stacked assembly of claim 19 wherein each of said attachment terminals includes either a bump or a well.

22. The stacked assembly of claim 21 wherein said bump is a gold stud bump.

23. The stacked assembly of claim 21 wherein said well is filled with solder.

24. The stacked assembly of claim 23 wherein said solder is indium-based.

25. The stacked assembly of claim 19 wherein said plurality of microelectronic elements includes at least one integrated circuit chip.

26. The stacked assembly of claim 19 wherein said plurality of microelectronic elements includes at least one chip containing integrated passive devices.

27. The stacked assembly of claim 19 wherein said plurality of microelectronic elements includes at least one chip for regulating or distributing power.

28. The stacked assembly of claim 19 wherein said plurality of microelectronic elements includes at least one test chip.

29. The stacked assembly of claim 19 wherein said multi-layer interconnection circuit comprises interconnection layers of metal conductors embedded in dielectric material.

30. The stacked assembly of claim 29 wherein selected ones of said metal conductors are shaped to form RF circuits in or on said dielectric material.

31. The stacked assembly of claim 19 wherein each of said delineated surfaces is dedicated to microelectronic elements of a single type: digital, analog, or radio frequency.

32. The stacked assembly of claim 19 wherein at least one of said attachment sites is used for attaching a cable.

33. The stacked assembly of claim 19 wherein each of said microelectronic elements is replaceable, prior to folding of said tabs.

34. A method for fabricating a stacked microelectronic assembly comprising the steps of:

a) providing an electrically conductive substrate;

b) providing a plurality of delineated surfaces in the plane of said conductive substrate;

c) fabricating a multi-layer interconnection circuit having conductive traces on said delineated surfaces;

d) providing one or more attachment sites on at least one of said delineated surfaces, each of said attachment sites including a plurality of attachment terminals, wherein each of said terminals may connect with a selected trace of said interconnection circuit;

e) attaching a plurality of microelectronic elements at said attachment sites using said attachment terminals;

f) providing a means to test said microelectronic elements by using a test chip at one of said attachment sites, or by using a cable connecting between one of said attachment sites and an external tester;

g) testing said microelectronic assembly using said test means and replacing any of said microelectronic elements that prove defective;

h) dicing said conductive substrate to separate said microelectronic assemblies if more than one of said assemblies is provided on said conductive substrate; and,

i) folding one or more of said delineated surfaces to form a stack of said delineated surfaces, for each of said microelectronic assemblies.

35. A rugged microelectronic assembly comprising:

a base substrate of copper;

an interconnection circuit fabricated on said base substrate;

one or more microelectronic assemblies attached to said interconnection circuit; and,

a top member of copper that is machined to accommodate any height variation in said assemblies.